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(54) Title: A WAFER-LEVEL MICRO-CAP PACKAGE AND METHOD OF MANUFACTURING THE SAME

(57) Abstract: A wafer-level micro-cap package consists of an assortment of small caps (16) molded onto a material with adjustable shapes and sizes to serve as protective structure against hostile environments associated with packaging or handling. It may also include a surface modification which enhances its adhesion to the MST wafer (12), and depending on the application, the molded cap (16) can be designed and modified to facilitate additional functions, such as optical, electrical, mechanical, and chemical, which are not easily achieved in the device by traditional means.

# A WAFER-LEVEL MICRO-CAP PACKAGE AND METHOD OF MANUFACTURING THE SAME

## Background of the Invention

*Related Applications*

The present application is related to U.S. Provisional Patent Application, serial no. 60/147,593, filed Aug. 5, 1999, which is herein incorporated by reference as if set out in its entirety.

*1. Field of the Invention*

The invention relates to the field of packaging microsystem technology (MST) devices associated with MST and microelectromechanical (MEMS) production, including semiconductor, micromachining, and biomedical fields. The present invention alleviates limitations in current MST "backend", package processing, improves the production throughput, and reduces the cost of MST packaging..

*2. Description of the Prior Art*

Microsystem technology devices (MSTs), which include micro-electro-mechanical-systems (MEMS), microelectro-mechanical-optical systems

(MEMOS), and other micromachined devices, have top surfaces which are very delicate. This is especially true with surface micromachined devices. Typically, there is great difficulty associated with taking a MST device from the wafer and packaging it into a deliverable product without causing irreversible damage to it in the process.

The manufacture and deployment of MSTs can be divided into two major steps: the front-end processing, where the structures are built in batch mode, typically on a wafer surface; and the back-end processing, where the devices are cut into individual dies, wire connections are made to a special package, and the package is sealed for protection. While front-end process development for MSTs has made tremendous progress recently by exploiting traditional integrated circuit (IC) processing techniques, the back-end packaging process is still problematic.

There are many limitations to using standard IC back-end package manufacturing tools and processes for packaging MSTs. Typical back-end processes for the IC industry include wafer dicing, device handling, die attachment, wire bonding and epoxy molding. All these processes induce some degrees of front-side device damage, yield loss, or device performance degradation. This clearly is the bottleneck in MST commercialization. An alternative MST device package process to ease these concerns is urgently needed.

## Brief Summary of the Invention

The invention is defined as an apparatus to facilitate the processing of microsystem technology devices in a packaging environment. The apparatus comprises a die on or in which the microsystem technology devices are fabricated, and a microcap having an upper surface and at least one contiguous descending wall connected to the die to provide a barrier to protect each of the microsystem technology devices from the packaging environment. In the preferred embodiment the microcap provides an enclosure completely surrounding the microsystem technology devices on the die. The enclosure provided by the microcap provides a sealed enclosure on five sides with a sixth side completing the enclosure being provided by the die.

The microcap is integrally molded with an interior shape to accommodate the microsystem technology devices on the die and to provide rugged protection and isolation of the microsystem technology devices from the packaging environment so that the die can be handled in the packaging environment without substantial risk of damage to the microsystem technology devices. The microcap is comprised of ceramic, metal, polymer or composites thereof. The microcap is arranged and configured to provide physical protection to the microsystem technology devices from the packaging environment and to provide a means of handling the die in the packaging environment without exposing the microsystem technology devices to damage.

In the preferred embodiment the apparatus comprises a wafer and a microcap layer in which a plurality of the dies are simultaneously and integrally fabricated together on and comprise the wafer, and in which a plurality of the microcaps are simultaneously and integrally fabricated together on and comprise the microcap layer. The microcap layer is adhesively connected to the wafer. The adhesive connection of the microcap layer and wafer is process enhanced, such as by means of partial curing of the microcap prior to connection to the wafer followed by completion of curing of the microcap after connection to the wafer; gas discharge treatment to modify contact surfaces of the microcap layer with the wafer, or adhesive coating of the microcap layer which is then placed in contact with the wafer. The sealed enclosure of the microcap is provided to the die is by means of a sealing process performed at a temperature below any possible damage to the microsystem technology devices.

The apparatus further comprises a device of additional functionality included in the microcap, such as an electromagnetic device, a microwave passive component, or electromagnetic interference shielding. The device of additional functionality may also comprise an optical device, such as an optical grating or a microlens.

The device of additional functionality may comprise a device which at least temporarily creates an environment for the microsystem technology devices at least simulative of an environment to which the microsystem technology devices are exposed as final packaged parts for quality control testing. In general the device of additional functionality comprises an optical, electrical, chemical or

mechanical means fabricated into the microcap to perform a predetermined function in addition to or in support of that performed by the microsystem technology devices.

In one embodiment of the invention the wafer has bonding pads defined therein and where the microcap layer is arranged and configured to include sacrificial segments, which when removed allow access to the bonding pads. while remaining portions of the microcap layer provide protection of the microsystem technology devices from the packaging environment and a means for handling of the dies.

The invention is also defined as a method to facilitate the processing of microsystem technology devices in a packaging environment comprising the steps of fabricating a die on or in which the microsystem technology devices are fabricated, fabricating a microcap having an upper surface and at least one contiguous descending wall connected to the die to provide a barrier to protect each of the microsystem technology devices from the packaging environment. and connecting the microcap to the die to place the barrier provided by the microcap between the microsystem technology devices and the packaging environment. The step of fabricating the microcap comprises fabricating the microcap by micromolding, such as by injection molding. hot embossing. or mold casting. The step of connecting the microcap to the die comprises sealing the microcap to the die at near-room temperature. The method further comprises the step of sealing each microcap to the die to enclose the microsystem technology devices.

The method further comprises the steps of integrally fabricating a wafer comprised of a plurality of the dies and integrally fabricating a microcap layer comprised of a plurality of the mircrocaps with at least one microcap corresponding to each one of the dies.

The method further comprises the steps of fabricating an optical. Electrical, chemical or mechanical elements into the microcap to perform a predetermined function in addition to or in support of that performed by the microsystem technology devices. The method in general further comprises the step of fabricating an optical, electrical, chemical or mechanical means into the microcap and at least temporarily creating by the optical, electrical, chemical or mechanical means an environment for the microsystem technology devices at least simulative of a final environment to which the microsystem technology devices are exposed as final packaged parts for quality control testing. The optical. Electrical, chemical or mechanical means is activated to simulate the final environment. The microsystem technology devices are then tested to determine their efficacy.

In one embodiment the method further comprises fabricating the microcap layer to include sacrificial segments disposed over bonding pads provided in the wafer, and selectively removing the sacrificial segments of the microcap layer to expose the bonding pads, while leaving other portions of the microcap layer to protect the microsystem technology devices and to provide a means for handling of dies. The wafer is separated into separate dies. The separate dies are

handled during subsequent packaging processes by means of the other portions of the microcap layer remaining with each die.

The invention has been described above in terms of means and steps for performing a function for the sake of grammatical ease, but it is to be expressly understood that the invention is not to be limited to the disclosed means or steps and their equivalents, but is to be construed to include all elements now known or later devised which are described by the words in the claims below. The invention now having been briefly summarized, an illustrated embodiment of the invention may be better visualized by turning to the following drawings wherein like elements are referenced by like numerals.

## Brief Description of the Drawings

Fig. 1 is a side cross-sectional view of a microcap layer of the invention on a wafer holding multiple MST devices.

Fig. 2 is a top plan view of a microcap layer of Fig. 1.

Fig. 3 is a side cross-sectional view of a single microcap of the invention mounted over a separate die or MST device.

Figs. 4a – 4j are side cross-sectional views of the process steps of a method whereby a microcap layer is manufactured by a molding process.

Figs. 5a-5c are side cross-sectional views illustrating adhesive enhancing steps whereby a microcap layer may be bonded to a wafer.

Fig. 6 is a side cross-sectional view illustrating adhesive mounting of a microcap or microcap layer to a wafer using an alignment jig.

Figs. 7a – 7d are side cross-sectional views illustrating how a microcap layer may be designed and used to facilitate wire bonding to dies in a wafer.

Fig. 8 is a side cross-sectional view diagram showing how the separate dies of Fig. 7d can be handled using conventional pick and place tooling.

Fig. 9 is a side cross-sectional diagram showing a single die which has been wire bonded after being handled by the process of Fig. 8.

The invention and its various embodiments can now be better understood by turning to the illustrated embodiment which is described by way of example in the following detailed description of the preferred embodiments.

**Detailed Description of the Preferred Embodiments**

The invention provides protection of the MST surface in the harsh environment associated with taking a MST device from a wafer pattern to a final packaged part. This protective device, which we call a "microcap", is inexpensive, customizable. and compatible with low temperature processing, which are all desirable features for this kind of invention. The invention provides a unique solution of introducing a low-temperature, wafer-level microcap for use as a temporary or permanent package to provide protection to MST devices in the hostile environment of back-end packaging.

A diagram of the invention is shown in Figs. 1 and 2, which are the side cross-sectional and top plan views respectively of an assembled wafer 12 with its

microcap layer 10. The diagram shows a thin patterned layer 10, called the microcap layer, composed of polymer, ceramic or metal material, which is bonded to the surface of a wafer 12 containing patterned MST devices or dies 14. This microcap layer 10, which may accommodate different die geometries, provides protection from the environment, and may include some additional functionality built into its design. Microcap layer 10 stays attached to wafer 12 throughout the packaging steps, and may be removed, if desired, at any time during the packaging process.

After wafer dicing, the each die 14 retains a piece of the microcap layer 10, namely its own microcap 16 as shown in Fig. 3. In this way, the microcap layer 10 and its subsequent separated microcap 16 provides an important link between front-end processing and the back-end packaging. By using this invention, standard automated packaging methods, such as vacuum pick-and place machines, may be employed, and the current bottleneck for MST production removed. The importance of this invention is very clear. It makes it possible to package MST devices or dies 14 with conventional automatic equipment.

A micro-molding technique, such as an injection molding, hot embossing, cast molding, or other methods, capable of dealing with a variety of desirable materials such as polymers, ceramics, and metals can be used to develop the wafer-level micro-cap layer 10 shown in Figs. 1 and 2. The wafer-level micro-cap layer 10 allows the use of low-cost planar molding processes, such as stamping, casting, for various sizes and shapes cap fabrication, and the use of low

temperature sealing processes for various kinds of MST devices 14, freeing specific requirements on the substrate materials housing MST devices 14. Furthermore, modification of micro-cap materials and design can be included to facilitate additional functionality such as hermetic sealing of MST devices 14, enhancing optical interfacing with MST devices 14, improving electrical performance of the MST devices 14 and the like. For example, a modification of the wafer-level microcap layer 10, having patterned metal thin/thick films coated on its surface, can be used for EMI shielding or spiral inductors in the microwave MST chips. This serves as an alternative to current IC processes which incorporate additional functions and components in microwave electronic chips ouch as microwave passive components , such as inductors and capacitors, and electromagnetic interference (EMI) shielding. This invention has no effect on front end processing of MSTs, and can be easily integrated with standard semiconductor IC package processes for MST chip packaging.

An adhesion-enhancing layer (not shown) may be used with microcap layer 10, and can render a leak-proof seal for MST devices 14 at the wafer level without degrading their performance. Depending on the strength of adhesion, microcaps 16 can serve as a temporary protective package for use through the standard packaging process, or may be used as a permanent package in the chip-on-board assembly. The strength of different adhesion-enhancing layers determines the whether microcaps 16 will be temporary or permanent. Various surface treatments such as gas discharge (plasma), radiation exposure, adhesion application, and chemical modification can be used to construct the adhesion

layer at low temperatures. The adhesion layer is responsible for enhancing surface adhesion between MST wafer 12 and the wafer-level micro-cap layer 10. Materials and adhesions can be customized to suit the particular application.

This invention allows MST production to be done on conventional automatic semiconductor IC packaging equipment. This is a major breakthrough to move MST devices 14 from high-end specialty applications to consumer markets. Furthermore, it can be exploited cheaply, quickly, and efficiently, and may even provide added functionality to the MST. In addition, this invention also allows an integration of MSTs 14 with other packaging technologies, such as low-profile, chip-on-board (COB) assembly, since it protects MST 14 from the glob-top epoxy used for COB encapsulation. In Table 1 below is a comparison illustrating the benefits of this invention.

TABLE 1

Overview of benefits of using microcap technology

| Process step | IC industry technique | Current MST industry technique | MST industry with invention |
|---|---|---|---|
| Wafer dicing | Automatic dicing saw | Automatic dicing saw Automatic dicing saw coated with PMMA and strip it one device at a time after dicing (otherwise, device will be damaged by the water jet or stiction may happen. | Automatic dicing saw |
| Device handling | Device Automatic pick-and-place | Manual, one device at a time | Automatic pick-and-place (biggest cost savings) |
| Wirebonding | Automatic | Automatic | Automatic |
| Epoxy molding | Automatic | None exist. Structures on surface will be damaged | Automatic |

| | | | |
|---|---|---|---|
| | | due to heat and pressure in molding. | |
| Testing | ATE for electrical | ATE available in final testing only | ATE for electrical, mechanical, optical can be done even in subassembly levels. |

Micro-cap 16 which protects the MST device or chips 14 may be constructed of various materials and with different sizes and shapes. Materials such as polymers, ceramics. metals may be used, depending on the application of MST device or chip 14. Microcaps 16 may be removed at any time during the packaging process, or may be a left on as a permanent part of MST device 14. A feature of the present invention is the fabrication of the wafer-level micro-cap layer 10, from a variety of materials, through a micro-molding process. The micro-molding technique may be any one of several conventional methods, including injection molding, hot embossing, and mold casting, and may deal with any kind of material. Any materials desired for microcap's specific application can be used to develop the wafer-level micro-cap layer 10. As a result of using the micro-molded microcap 16, the wafer level layer is sufficiently small in size and has a reliable means for protecting MST chips 14. In the preferred embodiment of the invention, a cast molding approach, using silicone rubber molds, is used to generate microcap layer 10 out of polymer. This is shown in Figs. 4a – 4j described below.

A second feature of the present invention is near-room temperature sealing of microcap 16 to various substrate materials containing MST devices 14.

The sealing may or may not be hermetic. This will ease MST device design for surface protection especially for high temperatures as well as reduce the potential damage of subjecting chip 14 to hostile outgassing environments. The sealing may be done by a variety of methods which enable adhesion between microcap layer 10 and substrate 12. This includes standard methods of modifying the surface adhesion properties, including gas discharge exposure, radiation exposure, chemical exposure, and the application of adhesives. Examples of adhesion are diagrammed in Figs. 5a – 5c. In the preferred embodiment of the invention, adhesive is stamped onto the surface of wafer 12 before sealing.

A third feature of the present invention is its flexibility which allows additional functional enhancement to microcap package 16 by geometric design of the package, material selection, or by modification of the microcap process. For example, it is well-known that the current IC processes for fabricating high quality passive components are complicated requiring multi-level interconnect metalization and planarization, while the use of additional discrete components in a printed circuit board prevents a compact system design for portable units. In this case, one can modify the cap process by having patterned metal thin/thick films coated on its surface for EMI shielding or spiral inductors in microwave MST chips 14. This serves as an alternative to current IC processes in incorporating additional functions and components in the microwave electronic chips 14 such as microwave passive components, like inductors and capacitors, and electromagnetic interference (EMI) shielding. Using a modified wafer-level

micro-cap layer 10, will ease not only the IC process constraints in producing the microwave components, but also component integration for a wafer level solution.

Another example is a modification of microcap 16 by having different microcap materials and microcap pattern designs which include optical elements. such as an optical grating or a micro-lens. This allows the microcap package 16 to better interface optical MST devices 14 with the optical signal. Depending on the microcap materials and design, addition functionality can be brought to microcap 16 for enhancing device performance, or providing new capabilities to MSTs 14.

A fourth feature of the present invention is its ability to mimic a final packaging environment. With proper design, microcaps 16 may temporarily mimic the operating environment of the final package, which allows wafer-level testing of the chips to be performed. This greatly facilitates quality control, since testing can be performed before packaging, saving potentially costly steps.

The advantages of the invention now having been outlined, turn now to the detailed steps of its implementation in the illustrated embodiment. It must be understood from the foregoing that many modifications can be made to the illustrated embodiment without departing from the scope of the invention. In a typical implementation, microcap layer 16 is manufactured after the die geometries have been determined for MSTs 14 on wafer 12. A mask (or several masks) is made for microcaps 16, and a micro-mold generated by standard micromachining processes. From this mold, microcap layers 10 are generated

which match the layout of MSTs 14 on wafer 12. This is diagrammed in the process steps shown in Figs. 4a – 4j. In Fig. 4a a substrate 18 is provide with a photoresist layer 20. It is patterned using a masked ultraviolet exposure at the step shown in Fig. 4b. At this point the desired patterned is transferred to the photoresist mask as shown in Fig. 4c. Substrate 18 is then deeply etched as shown at Fig. 4d and cleaned as shown in Fig. 4e leaving a master mold shape 18'. A mold casting 22 is then made against master mold shape 18' as shown in Fig. 4f. Mold casting 22 is then released from master mold shape 18' as shown in Fig. 4g. An opposing mold half 24 is then made by a similar process with the desired opposing mold shape and combined with mold casting 22 to provide a completed mold as shown in Fig. 4h. The material for microcap 16 is then disposed in the completed mold in Fig. 4h and mold casting 22 partially released and mounted on complete wafer 12 above devices 14 as shown in Fig. 4i. The shapes which are mold for microcap 16 are arbitrary and made according the requirements dictated by the MST design. After microcaps 16 are bonded to wafer 12, molding 24 is released leaving the assembled microcap 16 and substrate 12 as shown in Fig. 4j. Although a single device is illustrated in Figs. 4a – 4j, in practice, of course, multiple microcaps 16 are made and assembled to substrate 12 at one time to result in a microcap layer 10 on an MST wafer 12 with a corresponding multiplicity of separate MST devices 14.

After microcap layer 10 has been prepared, its surface may be modified to enhance adhesion to MST wafer 12. One way to ensure good adhesion is to perform an incomplete cure of the material in the mold, then remove from the

mold and complete the cure after contact has been made to wafer 12 as depicted in the diagram of Fig. 5a. Other methods include exposure of the material to gas discharge (for polymers) as depicted in the diagram of Fig. 5b, or direct application of adhesives to the surface as depicted in the diagram of Fig. 5c.

Alternately, adhesives may be patterned on wafer 12 as illustrated in Fig. 6. Microcap layer 10 is aligned with MSTs 14 on wafer 12. Alignment is facilitated with an alignment jig 26 and with alignment bosses or marks 28 on wafer 12 and microcap layer 10. After alignment has been achieved, microcap layer 10 is pressed into contact with wafer 12, and bonding allowed to occur. The surface treatments, such as creating an adhesion layer, should allow for low temperature bonding to occur. After bonding is complete, wafer 12 and microcap layer 10 may be removed from jig 26.

After microcap layer 10 has been bonded into place, wafer 12 may now continue with back-end processing without concern for damaging the delicate parts under microcap layer 10. All packaging steps, including wafer dicing, pick-and-place, epoxy molding, etc. may be performed without damaging MST device 14.

Microcap layer 10 may be specially designed to provide access to the bonding pads 30 as shown in Fig. 7. For a simple microcap layer design, several cuts may be made over the bonding pad regions to expose bonding pads 30 defined, for example, in a MEMOS wafer 36. These steps are illustrated in Figs. 7a – 7d. In Fig. 7a, microcap layer 10 is formed with protective portions 32 capping devices 14 and sacrificial segments 34 which provide access to

underlying bonding pads 30. As shown in Fig. 7b a dicing saw us used to open segments 34 by removing selected upper portions of microcap layer 10 to expose bonding pads 30 as shown in Fig. 7c. Wafer 36 is then diced in a conventional manner through bonding pads 30 according to design to provide separate dies 14 and microcaps 16 as shown in Fig. 7d mounted on an underlying Mylar adhesive tape 38. Dies 14 with their corresponding microcaps 16 may be then picked up with a conventional vacuum pick up tool 40 as shown in Fig. 8 and then moved to automated bonding and packing stations to be mounted on packaging 44 and wire bonded to a corresponding lead frame 42 with bonding wires 46 as shown in Fig. 9.

Microcap layers 10 may be designed to be functional elements, as well as protective devices. For example, optical elements, electrical elements, chemical and mechanical elements may be built into microcaps 16. For example, by coating microcaps 16 with a conductive layer, microcaps 16 may provide an electrical environment which is similar to the final packaged part, thus allowing accurate wafer level testing to be performed. Or, for example, special chemicals may be coated on the surface to react with biological agents and fluoresce, and the light emission may play a role in the MST device. Or, inductors can be patterned into microcaps 16 for added RF functionality. Or, optical elements such as lenses and gratings may be built into microcap 16 for improved optical coupling.

After dicing, each die 14 contains part of microcap layer 10 which still protects the device. Automated pick-and-place machines may handle the parts

without damaging MST device 14. The pieces may be glued to circuit boards and other packaging pieces without damage, or the entire MST may be encapsulated in a molded package. Microcap 16 may stay on the MST device 14 permanently, or if desired, microcap 16 may be removed before a final packaging piece is placed over MST 14.

Microcap 16 is easily and cheaply implemented and allows for the use of standard, mature packaging technologies. It flexible nature allows for the inclusion of new features and functionalities to add to the overall value of MST 14 which it protects.

Many alterations and modifications may be made by those having ordinary skill in the art without departing from the spirit and scope of the invention. Therefore, it must be understood that the illustrated embodiment has been set forth only for the purposes of example and that it should not be taken as limiting the invention as defined by the following claims. For example, notwithstanding the fact that the elements of a claim are set forth below in a certain combination, it must be expressly understood that the invention includes other combinations of fewer, more or different elements, which are disclosed in above even when not initially claimed in such combinations.

The words used in this specification to describe the invention and its various embodiments are to be understood not only in the sense of their commonly defined meanings, but to include by special definition in this specification structure, material or acts beyond the scope of the commonly defined meanings. Thus if an element can be understood in the context of this specification as including more than one meaning, then its use in a claim must be

understood as being generic to all possible meanings supported by the specification and by the word itself.

The definitions of the words or elements of the following claims are, therefore, defined in this specification to include not only the combination of elements which are literally set forth, but all equivalent structure, material or acts for performing substantially the same function in substantially the same way to obtain substantially the same result. In this sense it is therefore contemplated that an equivalent substitution of two or more elements may be made for any one of the elements in the claims below or that a single element may be substituted for two or more elements in a claim. Although elements may be described above as acting in certain combinations and even initially claimed as such, it is to be expressly understood that one or more elements from a claimed combination can in some cases be excised from the combination and that the claimed combination may be directed to a subcombination or variation of a subcombination.

Insubstantial changes from the claimed subject matter as viewed by a person with ordinary skill in the art, now known or later devised, are expressly contemplated as being equivalently within the scope of the claims. Therefore, obvious substitutions now or later known to one with ordinary skill in the art are defined to be within the scope of the defined elements.

The claims are thus to be understood to include what is specifically illustrated and described above, what is conceptionally equivalent, what can be obviously substituted and also what essentially incorporates the essential idea of the invention.

We claim:

1. An apparatus to facilitate the processing of microsystem technology devices in a packaging environment comprising:

a die on or in which said microsystem technology devices are fabricated; and

a microcap having an upper surface and at least one contiguous descending wall connected to said die to provide a barrier to protect each of said microsystem technology devices from said packaging environment.

2. The apparatus of claim 1 wherein said microcap provides an enclosure completely surrounding said microsystem technology devices on said die.

3. The apparatus of claim 2 wherein said enclosure provided by said microcap provides a sealed enclosure on five sides with a sixth side completing said enclosure being provided by said die.

4. The apparatus of claim 1 wherein said microcap is integrally molded with an interior shape to accommodate said microsystem technology devices on said die and to provide rugged protection and isolation of said microsystem technology devices from said packaging environment to allow said

die to be handled in said packaging environment without substantial risk of damage to said microsystem technology devices.

5. The apparatus of claim 1 further comprising a wafer and a microcap layer, wherein a plurality of said dies are simultaneously and integrally fabricated together on and comprise said wafer and wherein a plurality of said microcaps are simultaneously and integrally fabricated together on and comprise said microcap layer.

6. The apparatus of claim 5 wherein said microcap layer is adhesively connected to said wafer.

7. The apparatus of claim 6 wherein adhesive connection of said microcap layer and wafer is process enhanced.

8. The apparatus of claim 7 where said process enhanced connection between said microcap layer and wafer is by means of partial curing of said microcap prior to connection to said wafer followed by completion of curing of said microcap after connection to said wafer.

9. The apparatus of claim 7 where said process enhanced connection between said microcap layer and wafer is by means of a gas discharge treatment to modify contact surfaces of said microcap layer with said wafer.

10. The apparatus of claim 7 where said process enhanced connection between said microcap layer and wafer is by means of adhesive coating of said microcap layer which is then placed in contact with said wafer.

11. The apparatus of claim 3 wherein said sealed enclosure of said microcap is provided to said die is by means of a sealing process performed at a temperature below any possible damage to said microsystem technology devices.

12. The apparatus of claim 1 further comprising a device of additional functionality included in said microcap.

13. The apparatus of claim 12 where said device of additional functionality comprises an electromagnetic device.

14. The apparatus of claim 13 where said electromagnetic device comprises a microwave passive component.

15. The apparatus of claim 13 where said electromagnetic device comprises electromagnetic interference shielding.

16. The apparatus of claim 12 where said device of additional functionality comprises an optical device.

17. The apparatus of claim 16 where said optical device comprises an optical grating.

18. The apparatus of claim 16 where said optical device comprises a microlens.

19. The apparatus of claim 1 where said microcap is comprised of ceramic, metal, polymer or composites thereof.

20. The apparatus of claim 12 where said device of additional functionality comprises a device which at least temporarily creates an environment for said microsystem technology devices at least simulative of an environment to which said microsystem technology devices are exposed as final packaged parts for quality control testing.

21. The apparatus of claim 12 where said device of additional functionality comprises an optical, electrical, chemical or mechanical means fabricated into said microcap to perform a predetermined function in addition to or in support of that performed by said microsystem technology devices.

22. The apparatus of claim 1 where said microcap is arranged and configured to provide physical protection to said microsystem technology devices from said packaging environment and to provide a means of handling said die in said packaging environment without exposing said microsystem technology devices to damage.

23. The apparatus of claim 5 where said wafer has bonding pads defined therein and where said microcap layer is arranged and configured to include sacrificial segments, which when removed allow access to said bonding pads, while remaining portions of said microcap layer provide protection of said microsystem technology devices from said packaging environment and a means for handling of said dies.

24. A method to facilitate the processing of microsystem technology devices in a packaging environment comprising:

fabricating a die on or in which said microsystem technology devices are fabricated;

fabricating a microcap having an upper surface and at least one contiguous descending wall connected to said die to provide a barrier to protect each of said microsystem technology devices from said packaging environment; and

connecting said microcap to said die to place said barrier provided by said microcap between said microsystem technology devices and said packaging environment.

25. The method of claim 24 further comprising integrally fabricating a wafer comprised of a plurality of said dies and integrally fabricating a microcap layer comprised of a plurality of said mircrocaps, at least one microcap corresponding to each one of said dies.

26. The method of claim 24 further comprising sealing each microcap to said die to enclose said microsystem technology devices.

27. The method of claim 24 further comprising fabricating an optical, electrical, chemical or mechanical elements into said microcap to perform a predetermined function in addition to or in support of that performed by said microsystem technology devices.

28. The method of claim 24 further comprising:

fabricating an optical, electrical, chemical or mechanical means into said microcap and at least temporarily creating by said optical, electrical, chemical or mechanical means an environment for said microsystem technology devices at least simulative of a final environment to which said microsystem technology devices are exposed as final packaged parts for quality control testing;

activating said optical, electrical, chemical or mechanical means to simulate said final environment; and

testing said microsystem technology devices to determine their efficacy.

29. The method of claim 25 further comprising:

fabricating said microcap layer to include sacrificial segments disposed over bonding pads provided in said wafer;

selectively removing said sacrificial segments of said microcap layer to expose said bonding pads, while leaving other portions of said microcap layer to protect said microsystem technology devices and to provide a means for handling of dies;

separating said wafer into separate dies; and

handling said separate dies during subsequent packaging processes by means of said other portions of said microcap layer remaining with each die.

30. The method of claim 24 where fabricating said microcap comprises fabricating said microcap by micromolding.

31. The method of claim 24 where fabricating said microcap by micromolding comprises fabricating said microcap by injection molding, hot embossing, or mold casting.

32. The method of claim 24 where connecting said microcap to said die comprises sealing said microcap to said die at near-room temperature.

Figures for patent disclosure: A wafer-level microcap package

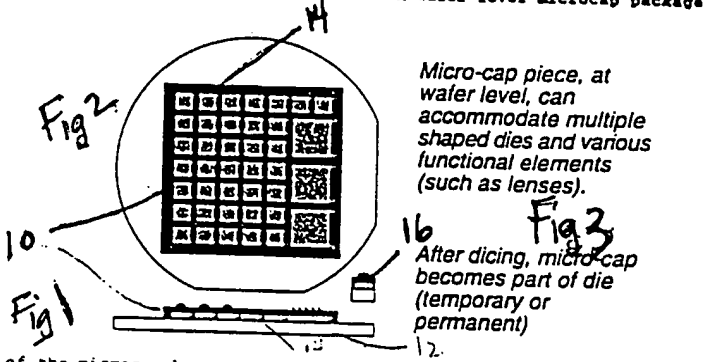
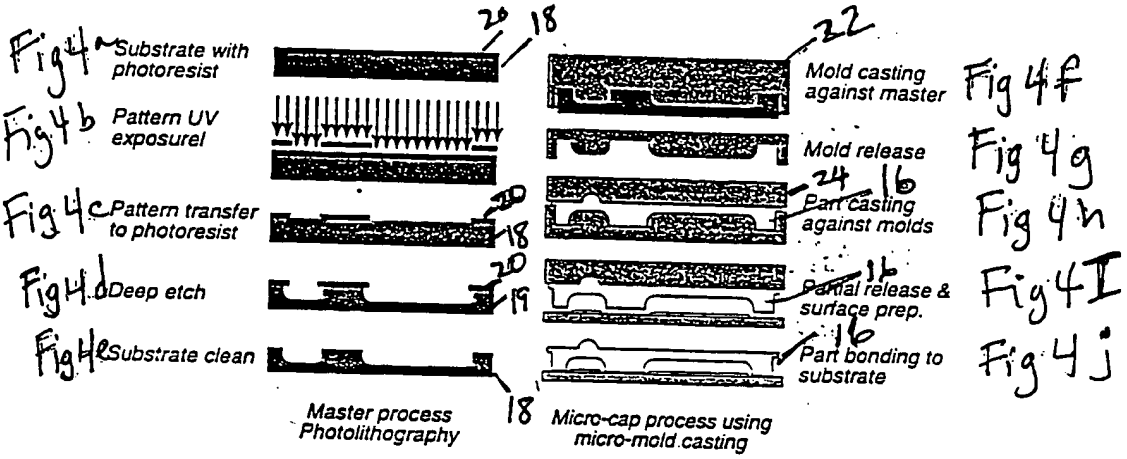



Figure 1: Diagram of the microcap layer and a microcap on a die. The microcap layer is designed to the needs of the MST devices, and may accommodate many different devices, and different MST designs. The microcap layer is bonded to the wafer before dicing. Testing of the chips may be done, and standard packaging processes may be performed without damaging the delicate MST chips. The microcaps may be removed before final packaging, if desired.



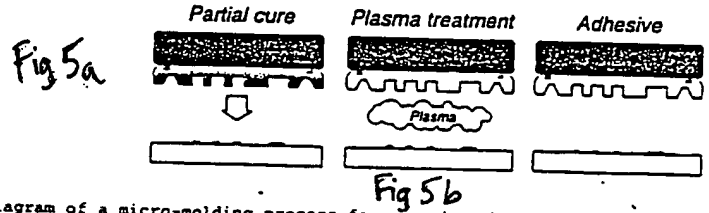




Figure 2a: Diagram of a micro-molding process for creating the microcap layer. The process uses standard microfabrication techniques to generate an inexpensive, temporary mold. This mold is used to generate the microcap layer.

Figure 2b: Diagram of three different methods for enhancing adhesion between the microcap layer and the MST substrate. "Partial cure" (left) removes a polymer from the cast mold before complete cure, then allows the micro-mold layer to compete cure on the wafer. Gas discharge treatment uses a plasma to modify the surface properties of the micro-mold. Adhesion coating applies adhesives to the micro-mold surface to promote bonding.

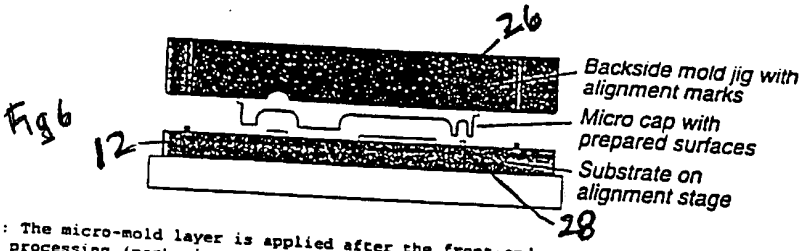



Fig 6

Figure 3: The micro-mold layer is applied after the front-end processing (micromachining) and before the back-end processing (packaging). An alignment tool is used with the micro-mold layer to place it in the correct location on the wafer.

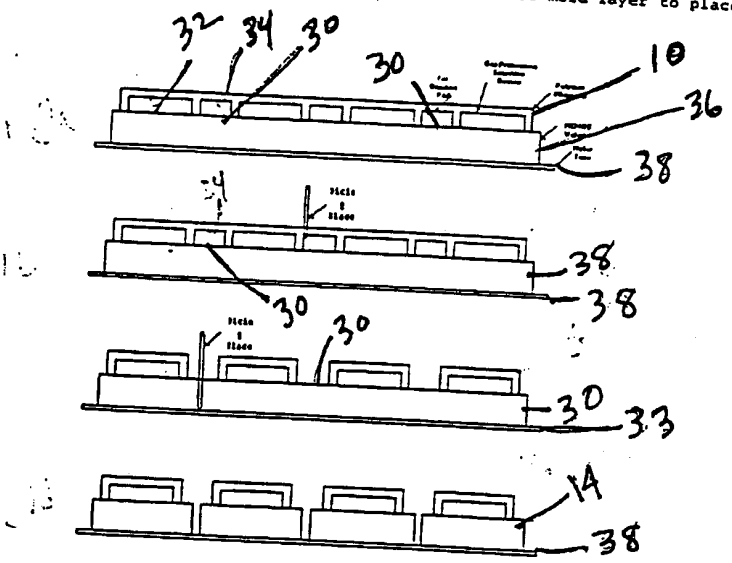



Fig 7 e

Figure 4: Demonstration of a simple method for opening up bonding pads from the microcap package. The dicing saw makes a "release pass" to open bonding regions, then makes the dicing cut through the wafer.

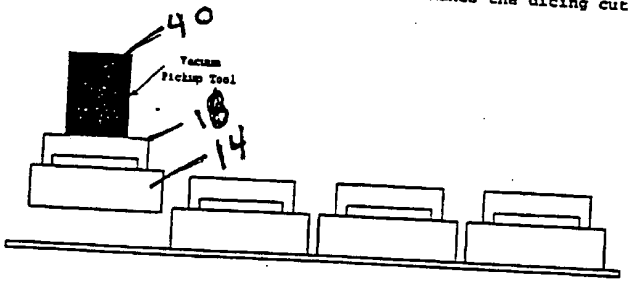



Fig 8

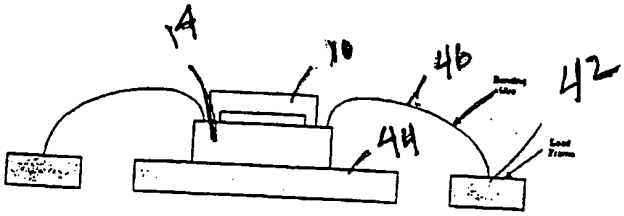



Fig 9

Figure 5: With microcap in place, MST dies may be handled, mounted, and wire bonded using conventional packaging equipment developed for the IC industry. The MST device will not be damaged.

# INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/21526

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) : B65B 47/00, H01L 23/12, H01L 21/48, H05K 3/30
US CL : 53/561, 128; 257/707; 438/112, 114, 118, 124, 127; 29/841
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 53/561, 128; 257/620, 707, ; 438/112, 114, 118, 124, 127; 29/840, 841

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category * | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | US 5,929,517 A (DISTEFANO et al.) 27 July 1999, See column 10, line 24-65 | 1-4, 11, 24, 26, 30-32 |
| X | US 5,353,498 A (FILLION et al.) 11 October 1994, See entire document. | 1-4, 11, 24-26, 29 |
| X | US 6,002,163 A (WOJNAROWSKI) 14 December 1999, See entire document. | 1-29 |

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

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